Abstract

A programmable logic device (PLD) includes a memory controller. The memory controller includes a first controller that communicates via a shared interface with a first memory external to the PLD. The memory controller also includes a second controller that communicates via the shared interface with a second memory external to the PLD. The PLD further includes an arbitration circuitry. The arbitration circuitry is configured to arbitrate ownership of the shared interface by the first and second controllers.